ATTY. DOCKET NO. WEST14-00018 PATENT

BACKPLANE ARCHITECTURE FOR USE IN WIRELESS AND WIRELINE ACCESS SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

The present invention is related to those disclosed in the following United States Provisional and Non-Provisional Patent Applications:

1) Serial No. 09/713,684, filed on November 15, 2000, entitled "SUBSCRIBER INTEGRATED ACCESS DEVICE FOR USE IN WIRELESS AND WIRELINE ACCESS SYSTEMS";

2) [Docket No. WEST14-00005] filed concurrently herewith, entitled "WIRELESS COMMUNICATION SYSTEM USING BLOCK FILTERING AND FAST EQUALIZATION-DEMODULATION AND METHOD OF OPERATION";

3) [Docket No. WEST14-00014], filed concurrently herewith, entitled "APPARATUS AND ASSOCIATED METHOD FOR OPERATING UPON DATA SIGNALS RECEIVED AT A RECEIVING STATION OF A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM";

4) [Docket No. WEST14-00015], filed concurrently herewith, entitled "APPARATUS AND METHOD FOR OPERATING A SUBSCRIBER INTERFACE IN A FIXED WIRELESS SYSTEM";

5) [Docket No. WEST14-00016], filed concurrently herewith, entitled "APPARATUS AND METHOD FOR CREATING SIGNAL AND

PROFILES AT A RECEIVING STATION";

6) [Docket No. WEST14-00017], filed concurrently herewith, entitled "SYSTEM AND METHOD FOR INTERFACE BETWEEN A SUBSCRIBER MODEM AND SUBSCRIBER PREMISES INTERFACES";

7) [Docket No. WEST14-00019], filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ON-LINE INSERTION OF LINE REPLACEABLE UNITS IN WIRELESS AND WIRELINE ACCESS SYSTEMS" ;

8) [Docket No. WEST14-00020], filed concurrently herewith, entitled "SYSTEM FOR COORDINATION OF TDD TRANSMISSION BURSTS WITHIN AND BETWEEN CELLS IN A WIRELESS ACCESS SYSTEM AND METHOD OF OPERATION";

9) [Docket No. WEST14-00021], filed concurrently herewith, entitled "REDUNDANT TELECOMMUNICATION SYSTEM USING MEMORY EQUALIZATION APPARATUS AND METHOD OF OPERATION";

10) [Docket No. WEST14-00022], filed concurrently herewith, entitled "WIRELESS ACCESS SYSTEM FOR ALLOCATING AND SYNCHRONIZING UPLINK AND DOWNLINK OF TDD FRAMES AND METHOD OF OPERATION";

11) [Docket No. WEST14-00023], filed concurrently herewith, entitled "TDD FDD AIR INTERFACE";

12) [Docket No. WEST14-00024], filed concurrently herewith, entitled "APPARATUS, AND AN ASSOCIATED METHOD, FOR PROVIDING WLAN SERVICE IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM";

13) [Docket No. WEST14-00026], filed concurrently herewith, entitled "WIRELESS ACCESS SYSTEM USING MULTIPLE MODULATION"];

14) [Docket No. WEST14-00027], filed concurrently herewith, entitled "WIRELESS ACCESS SYSTEM AND ASSOCIATED METHOD USING MULTIPLE MODULATION FORMATS IN TDD FRAMES ACCORDING TO SUBSCRIBER SERVICE TYPE";

15) [Docket No. WEST14-00028], filed concurrently herewith, entitled "APPARATUS FOR ESTABLISHING A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM";

16) [Docket No. WEST14-00029], filed concurrently herewith, entitled "APPARATUS FOR REALLOCATING COMMUNICATION RESOURCES TO ESTABLISH A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM";

17) [Docket No. WEST14-00030], filed concurrently herewith, entitled "METHOD FOR ESTABLISHING A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM";

18) [Docket No. WEST14-00033], filed concurrently herewith, entitled "SYSTEM AND METHOD FOR PROVIDING AN IMPROVED COMMON CONTROL BUS FOR USE IN ON-LINE INSERTION OF LINE REPLACEABLE UNITS IN WIRELESS AND WIRELINE ACCESS SYSTEMS";

19) Serial No. 60/262,712, filed on January 19, 2001, entitled "WIRELESS COMMUNICATION SYSTEM USING BLOCK FILTERING AND FAST EQUALIZATION-DEMODULATION AND METHOD OF OPERATION" [Docket No.

WEST14-00005];

20) Serial No. 60/262,825, filed on January 19, 2001, entitled "APPARATUS AND ASSOCIATED METHOD FOR OPERATING UPON DATA SIGNALS RECEIVED AT A RECEIVING STATION OF A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM" [Docket No. WEST14-00014];

21) Serial No. 60/262,698, filed on January 19, 2001, entitled "APPARATUS AND METHOD FOR OPERATING A SUBSCRIBER INTERFACE IN A FIXED WIRELESS SYSTEM" [Docket No. WEST14-00015];

22) Serial No. 60/262,827, filed on January 19, 2001, entitled "APPARATUS AND METHOD FOR CREATING SIGNAL AND PROFILES AT A RECEIVING STATION" [Docket No. WEST14-00016];

23) Serial No. 60/262,826, filed on January 19, 2001, entitled "SYSTEM AND METHOD FOR INTERFACE BETWEEN A SUBSCRIBER MODEM AND SUBSCRIBER PREMISES INTERFACES" [Docket No. WEST14-00017];

24) Serial No. 60/262,824, filed on January 19, 2001, entitled "SYSTEM AND METHOD FOR ON-LINE INSERTION OF LINE REPLACEABLE UNITS IN WIRELESS AND WIRELINE ACCESS SYSTEMS" [Docket No. WEST14-00019];

25) Serial No. 60/263,101, filed on January 19, 2001, entitled "SYSTEM FOR COORDINATION OF TDD TRANSMISSION BURSTS WITHIN AND BETWEEN CELLS IN A WIRELESS ACCESS SYSTEM AND METHOD OF OPERATION" [Docket No. WEST14-00020];

26) Serial No. 60/263,097, filed on January 19, 2001, entitled

"REDUNDANT TELECOMMUNICATION SYSTEM USING MEMORY EQUALIZATION APPARATUS AND METHOD OF OPERATION" [Docket No. WEST14-00021];

27) Serial No. 60/273,579, filed March 5, 2001, entitled "WIRELESS ACCESS SYSTEM FOR ALLOCATING AND SYNCHRONIZING UPLINK AND DOWNLINK OF TDD FRAMES AND METHOD OF OPERATION" [Docket No. WEST14-00022];

28) Serial No. 60/262,955, filed January 19, 2001, entitled "TDD FDD AIR INTERFACE" [Docket No. WEST14-00023];

29) Serial No. 60/262,708, filed on January 19, 2001, entitled "APPARATUS, AND AN ASSOCIATED METHOD, FOR PROVIDING WLAN SERVICE IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM" [Docket No. WEST14-00024];

30) Serial No. 60/273,689, filed March 5, 2001, entitled "WIRELESS ACCESS SYSTEM USING MULTIPLE MODULATION" [Docket No. WEST14-00026];

31) Serial No. 60/273,757, filed March 5, 2001, entitled "WIRELESS ACCESS SYSTEM AND ASSOCIATED METHOD USING MULTIPLE MODULATION FORMATS IN TDD FRAMES ACCORDING TO SUBSCRIBER SERVICE TYPE" [Docket No. WEST14-00027];

32) Serial No. 60/270,378, filed February 21, 2001, entitled "APPARATUS FOR ESTABLISHING A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM" [Docket No. WEST14-00028];

33) Serial No. 60/270,385, filed February 21, 2001, entitled "APPARATUS FOR REALLOCATING COMMUNICATION RESOURCES TO ESTABLISH A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM" [Docket No. WEST14-00029]; and

34) Serial No. 60/270,430, filed February 21, 2001, entitled "METHOD FOR ESTABLISHING A PRIORITY CALL IN A FIXED WIRELESS ACCESS COMMUNICATION SYSTEM" [Docket No. WEST14-00030].

The above applications are commonly assigned to the assignee of the present invention. The disclosures of these related patent applications are hereby incorporated by reference for all purposes as if fully set forth herein.

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to communication network access systems and, more specifically, to a backplane architecture for devices such as processors and modems used in wireless, cable, and wired voice frequency (VF) access systems.

BACKGROUND OF THE INVENTION

Telecommunications access systems provide for voice, data, and multimedia transport and control between the central office (CO) of the telecommunications service provider and the subscriber (customer) premises. Prior to the mid-1970s, the subscriber was provided phone lines (e.g., voice frequency (VF) pairs) directly from the Class 5 switching equipment located in the central office of the telephone company. In the late 1970s, digital loop carrier (DLC) equipment was added to the telecommunications access architecture. The DLC equipment provided an analog phone interface, voice CODEC, digital data multiplexing, transmission interface, and control and alarm remotely from the central office to cabinets located within business and residential locations for approximately 100 to 2000 phone line interfaces. This distributed access architecture greatly reduced line lengths to the subscriber and resulted in significant savings in both wire installation and maintenance. The reduced line lengths also improved communication performance on the line provided to the subscriber.

By the late 1980s, the limitations of data modem connections over voice frequency (VF) pairs were becoming obvious to both subscribers and telecommunications service providers. ISDN (Integrated Services Digital Network) was introduced to provide universal 128 kbps service in the access network. The subscriber

interface is based on 64 kbps digitization of the VF pair for digital multiplexing into high speed digital transmission streams (e.g., T1/T3 lines in North America, E1/E3 lines in Europe). ISDN was a logical extension of the digital network that had evolved throughout the 1980s. The rollout of ISDN in Europe was highly successful. However, the rollout in the United States was not successful, due in part to artificially high tariff costs which greatly inhibited the acceptance of ISDN.

More recently, the explosion of the Internet and deregulation of the telecommunications industry have brought about a broadband revolution characterized by greatly increased demands for both voice and data services and greatly reduced costs due to technological innovation and intense competition in the telecommunications marketplace. To meet these demands, high speed DSL (digital subscriber line) modems and cable modems have been developed and introduced. The digital loop carrier (DLC) architecture was extended to provide remote distributed deployment at the neighborhood cabinet level using DSL access multiplexer (DSLAM) equipment. The increased data rates provided to the subscriber resulted in upgrade DLC/DSLAM transmission interfaces from T1/E1 interfaces (1.5 Mbps to 2.0 Mbps) to high speed DS3 and OC3 interfaces. In a similar fashion, the entire telecommunications network backbone has undergone and is undergoing

continuous upgrade to wideband optical transmission and switching equipment.

Similarly, wireless access systems have been developed and deployed to provide broadband access to both commercial and residential subscriber premises. Initially, the market for wireless access systems was driven by rural radiotelephony deployed solely to meet the universal service requirements imposed by government (i.e., the local telephone company is required to serve all subscribers regardless of the cost to install service). The cost of providing a wired connection to a small percentage of rural subscribers was high enough to justify the development and expense of small-capacity wireless local loop (WLL) systems.

Deregulation of the local telephone market in the United States (e.g., Telecommunications Act of 1996) and in other countries shifted the focus of fixed wireless access (FWA) systems deployment from rural access to competitive local access in more urbanized areas. In addition, the age and inaccessibility of much of the older wired telephone infrastructure makes FWA systems a cost-effective alternative to installing new, wired infrastructure. Also, it is more economically feasible to install FWA systems in developing countries where the market penetration is limited (i.e., the number and density of users who can afford to pay for services is limited to a small percent of the population) and the rollout of

wired infrastructure cannot be performed profitably. In either case, broad acceptance of FWA systems requires that the voice and data quality of FWA systems must meet or exceed the performance of wired infrastructure.

Wireless access systems must address a number of unique operational and technical issues including:

1) Relatively high bit error rates (BER) compared to wire line or optical systems; and

2) Transparent operation with network protocols and protocol time constraints for the following protocols:

a) ATM;

b) Class 5 switch interfaces (domestic GR-303 and international V5.2);

c) TCP/IP with quality-of-service QoS for voice over IP (VoIP) (i.e., RTP) and other H.323 media services;

d) Distribution of synchronization of network time out to the subscribers;

3) Increased use of voice, video and/or media compression and concentration of active traffic over the air interface to conserve bandwidth;

4) Switching and routing within the access system to distribute signals from the central office to multiple remote cell

sites containing multiple cell sectors and one or more frequencies of operation per sector; and

5) Remote support and debugging of the subscriber equipment, including remote software upgrade and provisioning.

Unlike physical optical or wire systems that operate at bit error rates (BER) of 10^{-11}, wireless access systems have time varying channels that typically provide bit error rates of 10^{-3} to 10^{-6}. The wireless physical (PHY) layer interface and the media access control (MAC) layer interface must provide modulation, error correction, and automatic retransmission request (ARQ) protocol that can detect and, where required, correct or retransmit corrupted data so that the interfaces at the network and at the subscriber site operate at wire line bit error rates.

The wide range of equipment and technology capable of providing either wireline (i.e., cable, DSL, optical) broadband access or wireless broadband access has allowed service providers to match the needs of a subscriber with a suitable broadband access solution. However, in many areas, the cost of cable modem or DSL service is high. Additionally, data rates may be slow or coverage incomplete due to line lengths. In these areas and in areas where the high cost of replacing old telephone equipment or the low density of subscribers makes it economically unfeasible to introduce either DSL or cable modem broadband access, fixed

wireless broadband systems offer a viable alternative. Fixed wireless broadband systems use a group of transceiver base stations to cover a region in the same manner as the base stations of a cellular phone system. The base stations of a fixed wireless broadband system transmit forward channel (i.e., downstream) signals in directed beams to fixed location antennas attached to the residences or offices of subscribers. The base stations also receive reverse channel (i.e., upstream) signals transmitted by the broadband access equipment of the subscriber.

Unfortunately, the diversity of broadband access technology has resulted in a lack of standardization in the broadband access equipment. Cable modems and DSL routers are incompatible with each other and with fiber optic equipment. Different service providers locate broadband access equipment in different locations on the subscriber premises. Often this equipment is located inside the office or residence of the subscriber, which makes it inaccessible to maintenance workers unless the subscriber is present to admit the workers to the premises. The lack of standardization of broadband access equipment and the frequent inaccessibility of such equipment adds to the cost and complexity of broadband access.

Therefore, there is a need in the art for broadband access equipment that can be readily and inexpensively deployed in the large domestic and international markets that are not currently

served by wired or wireless broadband access technology. In particular, there is a need for broadband access equipment that provides competitive local exchange carriers (CLECs) a highly cost-effective turnkey facility solution that significantly improves profit margins and service quality. More particularly, there is a need for a subscriber integrated access device that may be easily and inexpensively installed and accessed at the subscriber's premises and that is compatible with different types of wireline and wireless broadband access technologies.

In particular, there is a need in the art for an improved backplane architecture for devices such as processors and modems that are used in wireline or wireless broadband access equipment.

SUMMARY OF THE INVENTION

To address the needs and deficiencies of the prior art, it is a primary object of the present invention to provide, for use in association with wireline or wireless broadband access equipment, an improved backplane for processors, modems and similar types of devices. According to an advantageous embodiment of the present invention, the improved backplane comprises a two tiered traffic and switching architecture that is capable of processing data at two different traffic rates. The improved backplane of the present invention may be used in more than one type of electronic equipment.

According to one advantageous embodiment of the present invention, the backplane is located within an access processor shelf.

According to another advantageous embodiment of the present invention, the backplane is located within a remote modem shelf.

According to still another advantageous embodiment of the present invention, the backplane is located within a unit that combines the functions of an access processor shelf and a remote modem shelf.

According to another advantageous embodiment of the present invention, the backplane further comprises a low tier that is capable of aggregate traffic rates of up to approximately two

gigabits per second (2 Gbps) and a high tier that is capable of aggregate traffic rates of up to approximately twenty gigabits per second (20 Gbps).

According to yet another advantageous embodiment of the present invention, the high tier of the backplane comprises a high tier bus comprising high speed serial links and at least one switch matrix card.

According to another advantageous embodiment of the present invention, the backplane further comprises additional bus structures including, without limitation, at least one of: a time division multiplex (TDM) bus, a communications bus, a common control bus, and a Joint Test Access Group (JTAG) test bus.

According to yet another advantageous embodiment of the present invention, the backplane comprises clocks and timing resources for use with backplane buses.

The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing

other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Before undertaking the DETAILED DESCRIPTION OF THE INVENTION below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances,

such definitions apply to prior, as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

FIGURE 1 illustrates an exemplary fixed wireless access network according to one embodiment of the present invention;

FIGURE 2 illustrates an exemplary access processor shelf comprising a backplane in accordance with the principles of the present invention;

FIGURE 3 illustrates an exemplary remote modem shelf comprising a backplane in accordance with the principles of the present invention;

FIGURES 4 illustrates a block diagram of an exemplary backplane of the present invention comprising a two-tiered traffic and switching architecture;

FIGURE 5 illustrates a block diagram of one advantageous embodiment of the exemplary backplane of the present invention showing the interconnection of the backplane with circuit board cards of an access processor shelf;

FIGURE 6 illustrates a block diagram of one advantageous embodiment of the exemplary backplane of the present invention showing the interconnection of the backplane with circuit board

cards of a remote modem shelf; and

FIGURE 7 illustrates a block diagram of one advantageous embodiment of the exemplary backplane of the present invention showing the interconnection of the backplane with circuit board cards of a unit that combines the functions of an access processor shelf and a remote modem shelf.

DETAILED DESCRIPTION OF THE INVENTION

FIGURES 1 through 7, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged subscriber integrated access device.

FIGURE 1 illustrates an exemplary fixed wireless access network 100 according to one embodiment of the present invention. Fixed wireless network 100 comprises a plurality of transceiver base stations, including exemplary transceiver base station 110, that transmit forward channel (i.e., downlink or downstream) broadband signals to a plurality of subscriber premises, including exemplary subscriber premises 121, 122 and 123, and receive reverse channel (i.e., uplink or upstream) broadband signals from the plurality of subscriber premises. Subscriber premises 121-123 transmit and receive via fixed, externally-mounted antennas 131-133, respectively. Subscriber premises 121-123 may comprise many different types of residential and commercial buildings, including single family homes, multi-tenant offices, small business enterprises (SBE), medium business enterprises (MBE), and so-called "SOHO" (small office/home office) premises.

The transceiver base stations, including transceiver base station 110, receive the forward channel (i.e., downlink) signals from external network 150 and transmit the reverse channel (i.e., uplink) signals to external network 150. External network 150 may be, for example, the public switched telephone network (PSTN) or one or more data networks, including the Internet or proprietary Internet protocol (IP) wide area networks (WANs) and local area networks (LANs). Exemplary transceiver base station 110 is coupled to RF remote modem shelf 140, which, among other things, up-converts baseband data traffic received from external network 150 to RF signals transmitted in the forward channel to subscriber premises 121-123. RF remote modem shelf 140 also down-converts RF signals received in the reverse channel from subscriber premises 121-123 to baseband data traffic that is transmitted to external network 150.

RF modem shelf 140 comprises a plurality of RF modems capable of modulating (i.e., up-converting) the baseband data traffic and demodulating (i.e., down-converting) the reverse channel RF signals. In an exemplary embodiment of the present invention, each of the transceiver base stations covers a cell site area that is divided into a plurality of sectors. In an advantageous embodiment of the present invention, each of the RF modems in RF modem shelf 140 may be assigned to modulate and demodulate signals in a

particular sector of each cell site. By way of example, the cell site associated with transceiver base station 110 may be partitioned into six sectors and RF modem shelf 140 may comprise six primary RF modems (and, optionally, a seventh spare RF modem), each of which is assigned to one of the six sectors in the cell site of transceiver base station 110. In another advantageous embodiment of the present invention, each RF modem in RF modem shelf 140 comprises two or more RF modem transceivers which may be assigned to at least one of the sectors in the cell site. For example, the cell site associated with transceiver base station 110 may be partitioned into six sectors and RF modem shelf 140 may comprise twelve RF transceivers that are assigned in pairs to each one of the six sectors. The RF modems in each RF modem pair may alternate modulating and demodulating the downlink and uplink signals in each sector.

RF remote modem shelf 140 is located proximate transceiver base station 110 in order to minimize RF losses in communication line 169. RF remote modem shelf 140 may receive the baseband data traffic from external network 150 and transmit the baseband data traffic to external network 150 via a number of different paths. In one embodiment of the present invention, RF remote modem shelf 140 may transmit baseband data traffic to, and receive baseband data traffic from, external network 150 through central office

facility 160 via communication lines 166 and 167. In such an embodiment, communication line 167 may be a link in a publicly owned or privately owned backhaul network. In another embodiment of the present invention, RF remote modem shelf 140 may transmit baseband data traffic to, and receive baseband data traffic from, external network 150 directly via communication line 168 thereby bypassing central office facility 160.

Central office facility 160 comprises access processor shelf 170. Access processor shelf 170 provides a termination of data traffic for one or more RF remote modem shelves, such as RF remote modem shelf 140. Access processor shelf 170 also provides termination to the network switched circuit interfaces and/or data packet interfaces of external network 150. One of the principal functions of access processor shelf 170 is to concentrate data traffic as the data traffic is received from external network 150 and is transferred to RF remote modem shelf 140. Access processor shelf 170 provides data and traffic processing of the physical layer interfaces, protocol conversion, protocol management, and programmable voice and data compression.

In an exemplary embodiment of the present invention shown in FIGURE 1, external network 150 is the public switched telephone network (PSTN). Remote modem shelf 140 transmits baseband data traffic to, and receives baseband data traffic from, access

processor shelf 170, which is located in central office facility 160 of the PSTN. Backhaul interface 145 of remote modem shelf 140 is coupled to backhaul interface 175 of access processor shelf 170 through communication line 167. Communication line 167 may comprise a radio frequency (RF) link, copper cable, optical fiber cable, or any other type of communication line data channel. Access processor shelf 170 is coupled to the public switched telephone network (PSTN) 150 through switch unit 165. Switch unit 165 comprises one or more data processing switches (not shown) such as packet switches or Class 5 switches.

It should be noted that network 100 was chosen as a fixed wireless network only for the purposes of simplicity and clarity in explaining the structure and operation of the backplane of the present invention. The choice of a fixed wireless network should not be construed in any manner that limits the scope of the present invention in any way. As will be explained below in greater detail, in alternate embodiments of the present invention, one or more backplanes of the present invention may be implemented in other types of broadband access systems, including wireline systems (i.e, digital subscriber line (DSL), cable modem, fiber optic, and the like) in which a wireline connected to a subscriber integrated access device carries forward and reverse channel signals.

FIGURE 2 illustrates exemplary access processor shelf 170

comprising backplane 210 in accordance with the principles of the present invention. Access processor shelf 170 performs a gateway function between the packet and switched circuit telecommunications networks 150 and remote modem shelf 140. Access processor shelf 170 provides data and traffic grooming of the physical layer interfaces, protocol conversion, protocol management, and programmable voice/data compression. Access processor shelf 170 supports "hot swap" or on-line replacement of all line replaceable units (e.g., circuit board cards) within access processor shelf 170.

FIGURE 2 illustrates an exemplary placement within backplane 210 of a plurality of circuit board cards 220, 230, ..., 280 of access processor shelf 170. Backplane 210 and circuit board cards 220, 230, ..., 280 are contained within a conventional chassis (not shown in FIGURE 2). The lower part of the chassis (under the circuit board cards) contains air ingress ports and a fan unit and the upper part of the chassis (above the circuit board cards) contains air egress ports and space for connecting cables. For ease of maintenance, circuit board cards 220, 230, ..., 280 may be inserted and removed from the front of the chassis.

Access processor shelf 170 comprises two DC power supply cards, 220 and 280. Power supply card 220 (and power supply card 280) coverts forty eight volts (48 V) to three and three

tenths volts (3.3 V), and to five volts (5 V) and to twelve volts (12 V) to provide the appropriate power level for the remaining circuit board cards of access processor shelf 170. The use of dual redundant power supply cards, 220 and 280, provides power backup in case one card fails.

Interface control processor (ICP) cards, 230 and 240, provide for shelf control functions, timing recovery and distribution, network interface, backhaul interface, protocol conversion, and resource queue management. Interface control processor (ICP) cards, 230 and 240, also provide a proxy manager for an element management system (EMS) (not shown) that manages control functions, monitor functions, alarm functions, etc. Interface control processor card 230 and interface control processor card 240 each comprise a network processor (not shown) that is capable of receiving software upgrades of network interface protocols.

Possible variants of interface control processor card architecture include: (1) Base line unit with dual T3/E3, octal T1/E1, and dual 10/100Base-T interfaces, and (2) Dual OC3 and dual 1000Base-T interfaces, and (3) Dual OC12 and quad 1000 Base-T interfaces. Although two interface control processor cards, 230 and 240, are shown in FIGURE 2, in other embodiments access processor shelf 170 may have more than two interface control processor cards.

Signal processing (SP) card 250 provides synchronous voice compression, emergency 911 "cut through"/redial (emergency service), and access network (AN) call progress tone generation and tone detection.

Switch matrix (SM) cards, 260 and 270, provide switching and redundancy support for OC3/OC12 ICP cards, 230 and 240. Although two switch matrix cards, 260 and 270, are shown in FIGURE 2, in other embodiments access processor shelf 170 may have more than two switch matrix cards.

Backplane 210 connects all of the above described circuit board cards 220, 230, ..., 280. As will be more fully described, backplane 210 comprises a dual redundant bus structure and high speed serial star buses that are scalable to OC12 (655 Mbps) / OC48 (2.4x Gbps) transport to redundant switch matrix (SM) cards, 260 and 270.

FIGURE 3 illustrates exemplary remote modem shelf 140 comprising backplane 210 in accordance with the principles of the present invention. Remote modem shelf 140 terminates the compressed and concentrated backhaul link of communication line 167 from access processor shelf 170 and routes the traffic to the appropriate radio frequency (RF) modem card for communication through transceiver base station 110 to the appropriate subscriber premises. In one advantageous embodiment remote modem shelf 140

provides support for up to six (6) cell sectors of transceiver base station 110. Remote modem shelf 140 supports "hot swap" or on-line replacement of all line replaceable units (e.g., circuit board cards) within remote modem shelf 140.

FIGURE 3 illustrates an exemplary placement within backplane 210 of a plurality of circuit board cards 320, 330, ..., 370 of remote modem shelf 140. Backplane 210 and circuit board cards 320, 330, ..., 370 are contained within a conventional chassis (not shown in FIGURE 3). The lower part of the chassis (under the circuit board cards) contains air ingress ports and a fan unit and the upper part of the chassis (above the circuit board cards) contains air egress ports and space for connecting cables. For ease of maintenance, circuit board cards 320, 330, ..., 370 may be inserted and removed from the front of the chassis.

Remote modem shelf 140 comprises two DC power supply cards, 320 and 370. Power supply card 320 (and power supply card 370) coverts forty eight volts (48 V) to three and three tenths volts (3.3 V), and to five volts (5 V) and to twelve volts (12 V) to provide the appropriate power level for the remaining circuit board cards of remote modem shelf 140. The use of dual redundant power supply cards, 320 and 370, provides power backup in case one card fails.

Remote modem shelf 140 contains interface control processor

(ICP) cards, 330 and 340. In a manner similar to that of the interface control processor cards, 230 and 240, in access processor shelf 170, interface control processor cards, 330 and 340, provide for shelf control functions, timing recovery and distribution, network interface, backhaul interface, protocol conversion, and resource queue management. Interface control processor (ICP) cards, 330 and 340, also provide a proxy manager for an element management system (EMS) (not shown) that manages control functions, monitor functions, alarm functions, etc. Interface control processor card 330 and interface control processor card 340 each comprise a network processor (not shown) that is capable of receiving software upgrades of network interface protocols. Although two interface control processor cards, 330 and 340, are shown in FIGURE 3, in other embodiments remote modem shelf 140 may have more than two interface control processor cards.

Radio frequency (RF) modem cards, 350 and 360, support aggregate data rates from ten million bits per second (10 Mbps) to one hundred fifty five million bits per second (155 Mbps). The baseband modems of RF modem cards, 350 and 360, use "software radio" architecture and are capable of supporting two (2) simultaneous air interfaces for staged change over to alternate air interfaces that are in the standards process (e.g., IEEE 802.16.3).

Possible variants of frequency utilization that can be supported with RF modem cards, 350 and 360, include: (1) 2.5 GHz to 2.7 GHz ITFS/MMDS, and (2) 5.8 GHz UNII unlicensed band (Tier 3 and Tier 4 markets), (3) 3.4 GHz to 3.7 GHz international fixed wireless access (FWA) band and later domestic employment, and (4) 4.9 GHz domestic fixed wireless. Although two RF modem cards, 350 and 360, are shown in FIGURE 3, in other embodiments remote modem shelf 140 may have more than two RF modem cards.

Interface control processor cards, 330 and 340, are also used for control and routing functions and provide both timing and critical time division duplex (TDD) coordinated burst timing for radio frequency (RF) modem cards, 350 and 360 (and for all other RF modem cards that are located within remote modem shelf 140). Interface control processor cards, 330 and 340, also provide shelf to shelf timing for stacked frequency high density cell configurations. Given the remote deployment of remote modem shelf 140, special care must be given to thermal density and thermal management for remote modem shelf 140.

Backplane 210 connects all of the above described circuit board cards 320, 330, ..., 370. As will be more fully described, backplane 210 comprises a dual redundant bus structure and high speed serial star buses.

FIGURE 4 illustrates a block diagram of exemplary

backplane 210 of the present invention comprising a two-tiered traffic and switching architecture. Exemplary backplane 210 shown in FIGURE 4 is located within access processor shelf 170.

The low tier of backplane 210 comprises low tier bus 410. Low tier bus 410 supports aggregate traffic rates of up to approximately two gigabits per second (2 Gbps). Low tier bus 410 is based on a CellBus™ distributed switching architecture. CellBus™ is a trademark of TransSwitch Corporation. Low tier bus 410 is the principal communications path between interface control processor (ICP) cards, 230 and 240, and signal processing cards/auxiliary processing cards, 460, 465 and 470 in access processor shelf 170. In remote modem shelf 140, low tier bus 410 is the principal communications path between interface control processor (ICP) cards, 330 and 340, and RF modem cards, 350 and 360.

Low tier bus 410 provides support for asynchronous transfer mode (ATM) cell-based traffic between appropriately equipped cards within backplane 210. Low tier bus 410 is a parallel bus architecture consisting of a thirty two (32) bit data path and associated control signaling. Low tier bus 410 can support a mix of unicast, multicast, and broadcast traffic. Low tier bus 410 provides a switch fabric across backplane 210 by (1) allowing any appropriately equipped card on the input side of the connection to transmit data to any appropriately equipped card on the output side

of the connection, and by (2) allowing any appropriately equipped card on the output side of the connection to receive data transmitted from any appropriately equipped card on the input side of the connection.

Low tier bus 410 wraps ATM cells with an additional header and with parity in order to switch cell based traffic according to a connection map maintained by software on each circuit board card. Low tier bus 410 is also capable of supporting packet based traffic.

Low tier bus 410 utilizes GTLP drivers that are pulled up on backplane 210. The abbreviation GTLP stands for "GTL+" or "gunning transistor logic plus." Low tier bus 410 is referenced to one half of the fundamental 65.536 MHz backplane clock. Therefore, low tier bus 410 operates at a nominal clock rate of 32.768 MHz. Two phases of the 65.536 MHz clock bus are provided by primary and secondary timing masters to accommodate the timing requirements of low tier bus 410. Backplane 210 provides full redundancy of low tier bus 410 in the form of two complete sets of data/control signals. A redundant clock reference for low tier bus 410 is also provided.

The high tier of backplane 210 comprises high tier bus 415 and switch matrix cards, 260 and 270. High tier bus 415 supports aggregate traffic rates of up to approximately twenty gigabits per second (20 Gbps). High tier bus 415 uses redundant high speed

serial links in conjunction with dedicated switch matrix cards, 260 and 270.

High speed serial links provide high capacity transport of user and control traffic between the appropriate card types (e.g., OC-3N) and switch matrix cards, 260 and 270. The high speed serial links are point-to-point serial links comprising differential pairs for both a transmit path and a receive path. Traffic on the high speed serial links terminates at switch matrix card 260 (or switch matrix card 270) where uniform length traffic is switched to an appropriate backplane card slot in accordance with the information contained within each cell's header.

The high speed serial links are differential low voltage positive emitter coupled logic (LVPECL) levels that are driven from source to destination and are terminated on the receiving end of links. The links are referenced to the 65.536 MHz clock reference that is provided by primary and secondary master timing interface control processor (ICP) cards. This clock rate is multiplied by twenty (20) by the high speed serial link serial/de-serial devices (SERDES devices) to provide a baud rate of 1.31072 MHz. Because each link is 8B/10B encoded, the corresponding transmission rate is approximately 1.05 Gbps. In another advantageous embodiment of the present invention, the transmission rate is approximately 2.5 Gpbs.

The high speed serial links are redundant in that there is a

minimum of two (2) links per ICP slot. One transmit/receive pair terminates at switch matrix card 260 (on the A side) and the other transmit/receive pair terminates at switch matrix card 270 (on the B side).

The data transmitted by the high speed serial links are 8B/10B encoded, but no parity checks are made at the PHY level. However, any data traffic sent across the high speed serial links will be CRC checked (cyclic redundancy checked) across the cell/packet level. Consequently, the integrity of each high speed serial link is verified with each cell/packet transfer. Because each high speed serial link is a point-to-point topology, no fault isolation is necessary.

As shown in FIGURE 4, interface control processor cards, 230 and 240, are coupled to and communicate with both low tier bus 410 and high tier bus 415. Interface control processor card 230 comprises data shaping and grooming unit 435 and line interface 440. Similarly, interface control processor card 240 comprises data shaping and grooming unit 450 and line interface 455. Interface control processor cards, 230 and 240, also are coupled to and communicate with switch matrix card 260 and with switch matrix card 270. Signal processing cards/auxiliary processing cards, 460, 465 and 470, are coupled to and communicate with low tier bus 410 and with high tier bus 415.

The two-tiered traffic and switching architecture of the backplane of the present invention has been described with reference to backplane 210 within access processor shelf 170. However, the same two-tiered traffic and switching architecture of the present invention is utilized in backplane 210 within remote modem shelf 140. In addition, the two-tiered traffic and switching architecture of the backplane of the present invention may also be utilized within a backplane 210 within a unit that combines the functions of access processor shelf 170 and remote modem 140.

Other advantageous embodiments of backplane 210 within access processor shelf 170 and other advantageous embodiments of backplane 210 within remote modem shelf 140 (and other advantageous embodiments of backplane 210 within a unit that combines the functions of access processor shelf 170 and remote modem shelf 140) comprise additional bus structures.

For example, an additional advantageous embodiment of backplane 210 may comprise (in addition to low tier bus 410 and high tier bus 415) a time division multiplex (TDM) bus, a communications bus, a common control bus, a Joint Test Access Group (JTAG) test bus, and clocks and framing resources.

A time division multiplex (TDM) bus provides a resource that is especially suitable for interfacing with legacy circuit-switched network interfaces. A time division multiplex (TDM) bus comprises

thirty two (32) independent serialized buses, each of which carries voice or data traffic, channelized into a DS0 format. A TDM bus provides a switch fabric across backplane 210 by (1) allowing any TDM-equipped card on the input side of the connection to transmit within specified time slots, and by (2) allowing any TDM-equipped card on the output side of the connection to receive the data within the corresponding time slots.

An exemplary TDM bus within backplane 210 utilizes GTLP drivers that are pulled up on backplane 210. Each TDM bus is designed to operate at a rate of either 8.192 Mbps or 16.384 Mbps. When all cards within backplane 210 are operating at the rate of 8.192 Mbps, then two thousand forty eight (2,048) full duplex DS0 channels are supported by the TDM bus. When all cards within backplane 210 are operating at the rate of 16.384 Mbps, then four thousand ninety six (4,096) full duplex DS0 channels are supported by the TDM bus. The TDM bus is also capable of simultaneously operating with a mix of cards where some cards operate at 8.192 Mbps and where some cards operate at 16.384 Mbps.

Each of the thirty two (32) serial buses that make up the TDM bus operates independently of the remaining serial buses. Consequently, if one of the thirty two (32) serial buses fails (e.g., due to a component failure with an ICP card) it is possible (depending upon the type of failure) that the remaining thirty one

(31) serial buses of the TDM bus will not be affected. However, to assure full redundancy, a second TDM bus with a second set of thirty two (32) serial buses is provided. The second TDM bus can either be operated in standby mode for full redundancy, or operated in active mode to double the TDM bus capacity on backplane 210.

A communications bus comprises a serial bus that supports general communications between circuit board cards of backplane 210. A communications bus also supports specialized communications for system redundancy purposes. Communications bus of backplane 210 is a backplane version of the IEEE-1394 serial bus standard. The communications bus on backplane 210 utilizes GTLP drivers that are pulled up on backplane 210. The communications bus is referenced to 100 MHz local oscillators located on each card within backplane 210.

A common control bus is a serial bus that supports control and maintenance functions. The control and maintenance functions supported by a control bus include: (1) periodic alarm and maintenance scanning of each card slot, and (2) validation of card type and revision level prior to bringing a card into service, and (3) reset control of each card slot. An advantageous embodiment of a common control bus utilizes the I^2C protocol described in "The I^2C Bus Specification" published by Philips Semiconductor. The term "I^2C Bus" is a shorthand expression for "Inter Integrated Circuit

Bus."

The common control bus within backplane 210 utilizes GTLP drivers that are pulled up on backplane 210. The common control bus operates in a multi-master mode and is self-clocked by the master controller. Backplane 210 provides full redundancy for the common control bus in the form of two (2) complete sets of data/control signals.

The common control bus within backplane 210 has no inherent facilities for detecting the occurrence of a failure (e.g., that a bus is held "low"). Therefore, a means for detecting failures on the common control bus is required. One possible method for testing the integrity of the common control bus is to periodically read data from a well known address space (e.g., the EEPROM for backplane 210).

A Joint Test Access Group (JTAG) test bus is a bused version of the IEEE 1149 standard. A JTAG test bus is used to provide a card-level test interface for each card slot. Each card in access processor shelf 170 (and each card in remote modem shelf 140) incorporates an IEEE 1149 transceiver that isolates each card until the address that corresponds to the card slot is received from an IEEE 1149 test master.

The JTAG test bus within backplane 210 uses standard transistor transistor logic (TTL) levels, which (except for the

return data path) are driven by an IEEE 1149 bus master. The operation of the JTAG test bus of backplane 210 assumes that the IEEE 1149 bus master is an external device. All clocking and messaging of the JTAG test bus are controlled by the external tester.

Clocks and framing resources of backplane 210 provide the timing for the synchronous time division multiplex (TDM) resources. The timing signals consist of (1) a 65.536 MHz clock signal referenced to a network qualified source, and (2) an eight kiloHertz (8 kHz) frame signal that is phase locked to the 65.536 MHz clock signal. The 65.536 MHz clock is also utilized as reference timing for low tier bus 410 (CellBus™) and for high tier bus 415 (high speed serial links). This allows the derivation of clocks synchronous with the network. The clock signals are differential signals transmitted from the primary (and secondary) timing masters to remaining card slots.

Separate sets of clock and framing resources are provided on backplane 210. The first set of clock and framing resources is driven by a primary master interface control processor (ICP) card. The second set of clock and framing resources is driven by a secondary master interface control processor (ICP) card. Under normal operation, the two clocks should be derived (as directed by software control) from the same reference source. Consequently, the

two sets of clock and framing resources are phase locked. This allows individual interface control processor (ICP) cards to switch traffic between the two TDM buses in an error free manner.

Each card contains circuitry for detecting a missing clock signal in order to allow an error free switchover to a redundant set of clock and framing resources.

The bus structures described above may be incorporated into a backplane architecture within access processor shelf 170, or within remote modem shelf 140, or within a unit that combines the functions of access processor shelf 170 and remote modem shelf 140.

FIGURE 5 illustrates exemplary backplane 210 within access processor shelf 170 comprising low tier bus 410 (CellBus™), high tier bus 415 (high speed serial link), time division multiplex (TDM) bus 510, communications bus 520, common control bus 530, and clocks and framing resources 540. The designation (A/B) signifies that each bus is a dual bus with a first A side and a second B side. FIGURE 5 illustrates an exemplary access processor shelf 170 in which all twenty one (21) card slots are fully populated. Each of the individual circuit board cards within the twenty one (21) card slots are capable of accessing each of the buses on backplane 210 (including buses on backplane 210 not shown in FIGURE 5).

FIGURE 6 illustrates exemplary backplane 210 within remote modem shelf 140 comprising low tier bus 410 (CellBus™), high tier

bus 415 (high speed serial link), time division multiplex (TDM) bus 610, communications bus 620, common control bus 630, and clocks and framing resources 640. The designation (A/B) signifies that each bus is a dual bus with a first A side and a second B side. FIGURE 6 illustrates an exemplary remote modem shelf 140 in which all twenty one (21) card slots are fully populated. Each of the individual circuit board cards within the twenty one (21) card slots are capable of accessing each of the buses on backplane 210 (including buses on backplane 210 not shown in FIGURE 6).

FIGURE 7 illustrates exemplary backplane 210 within a unit combining the functions of access processor shelf 170 and remote modem shelf 140 comprising low tier bus 410 (CellBus™), high tier bus 415 (broad band switch serial bus), modem bus 710, control bus 720, control/alarm bus 730 (including JTAG bus), and clocks and framing resources 740. The designation (A/B) signifies that each bus is a dual bus with a first A side and a second B side. Each of the individual circuit board cards within the twenty one (21) card slots are capable of accessing each of the buses on backplane 210 (including buses on backplane 210 not shown in FIGURE 7).

The examples of backplane 210 set forth above show how the improved backplane architecture of the present invention may be used in more than one type of electronic device. The examples set forth above also show that an advantageous embodiment of backplane

210 may comprise of all of the bus structures and clock and framing resources described in this patent document.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.